Challenges and Opportunities of III-V Nanoelectronics for Future Logic Applications

Robert Chau

Intel Senior Fellow

Director of Transistor Research and Nanotechnology

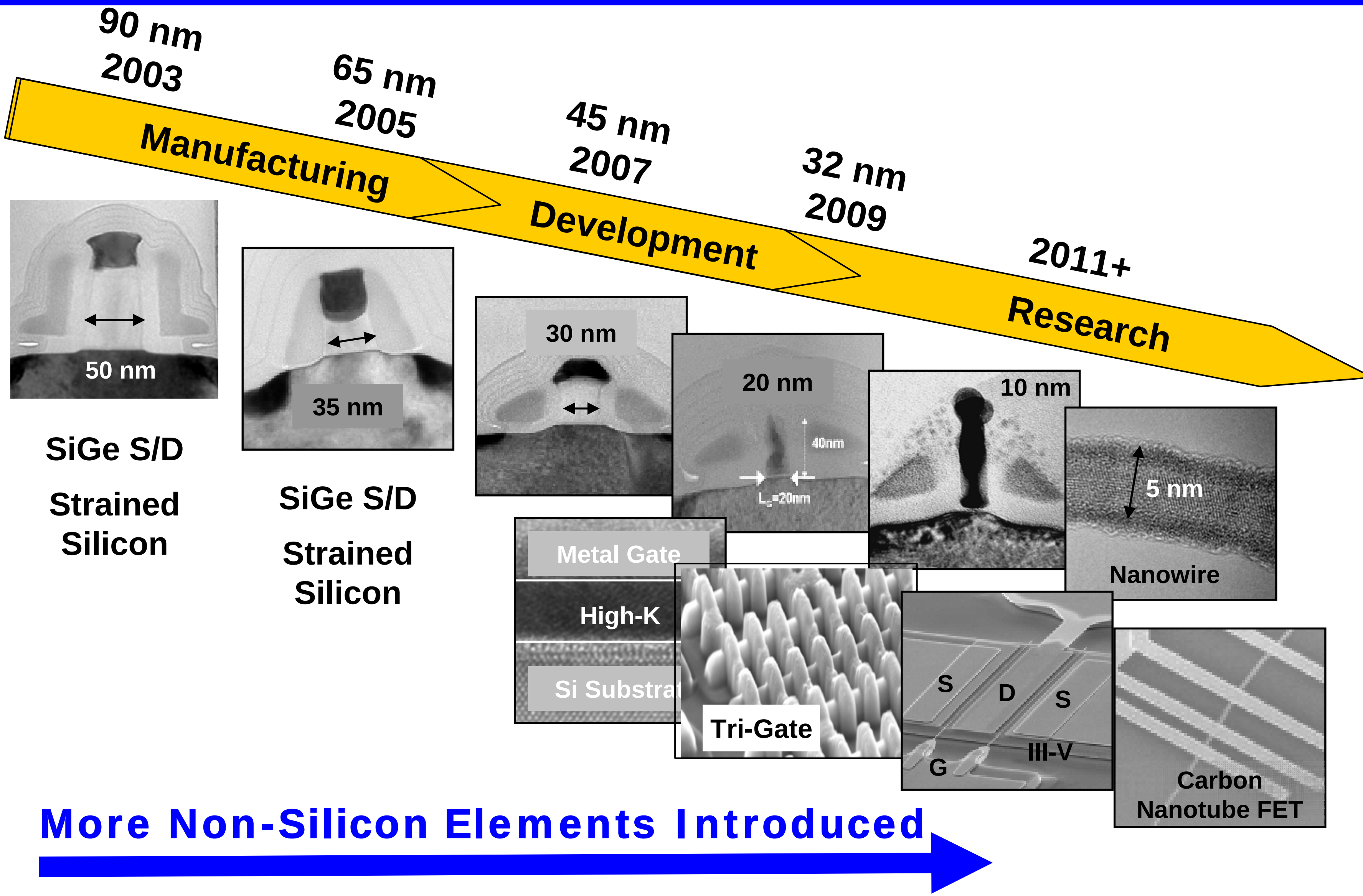
Intel Corporation

June 26, 2006

Content

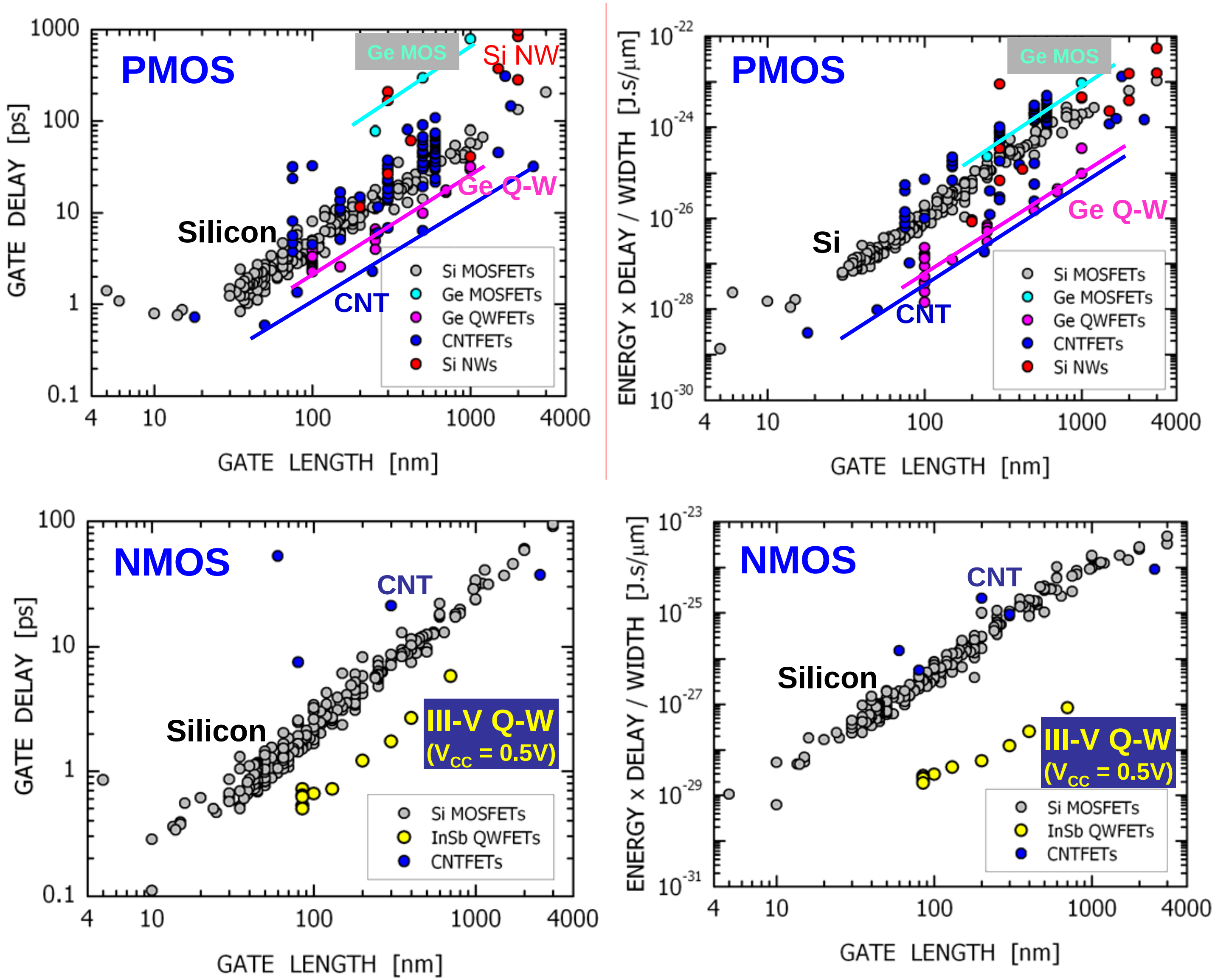
- Emerging non-Si nanoelectronic devices
- Why III-V nanoelectronics research ?
- Performance of III-V quantum-well devices at 0.5V
- Challenges and opportunities of III-V for future high-speed and low-power CMOS applications

Transistor Nanotechnology

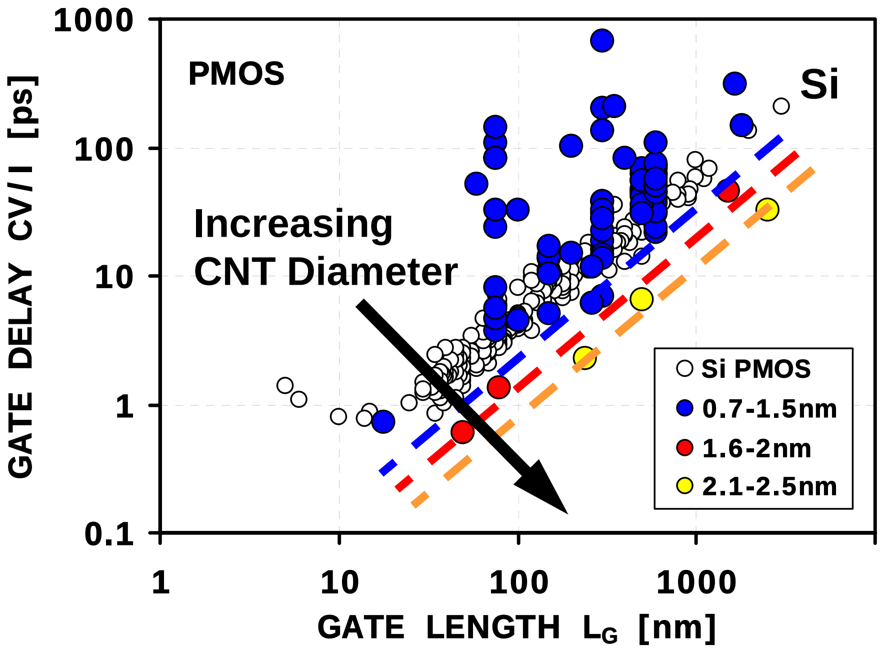


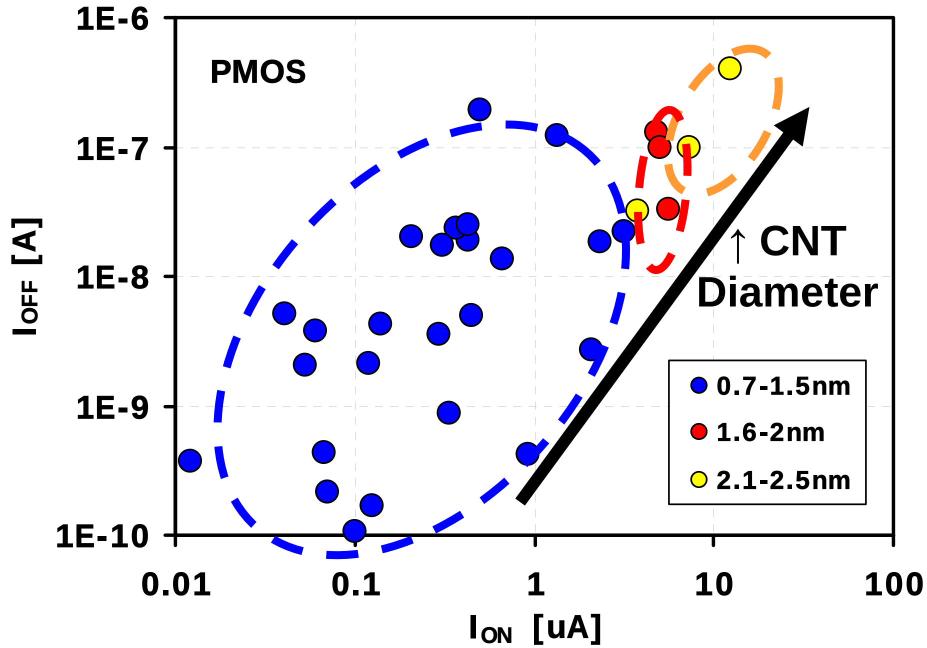
Future options subject to change

Emerging Non-Si Device Research



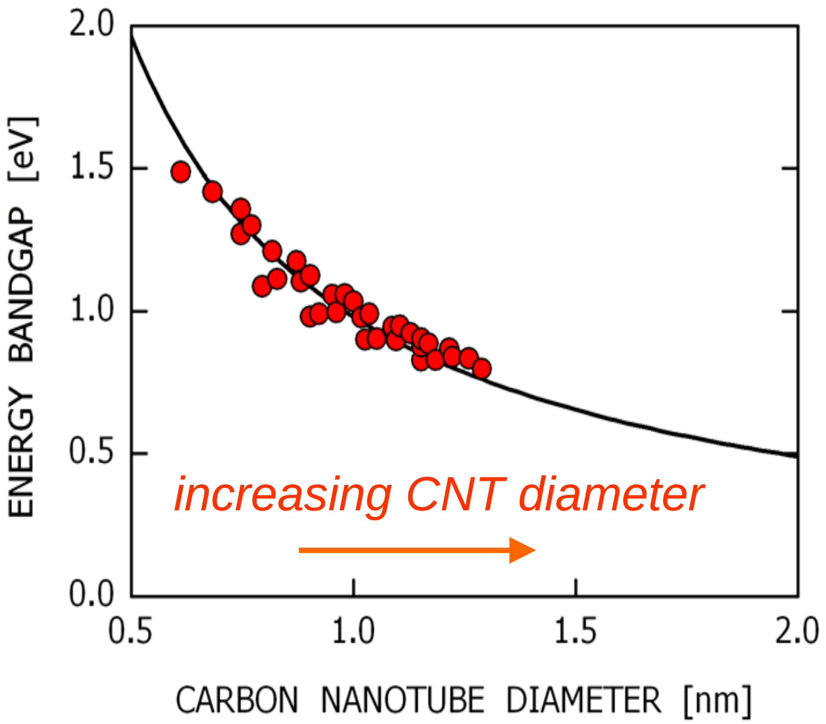
Emerging Device: Carbon Nanotube Transistor

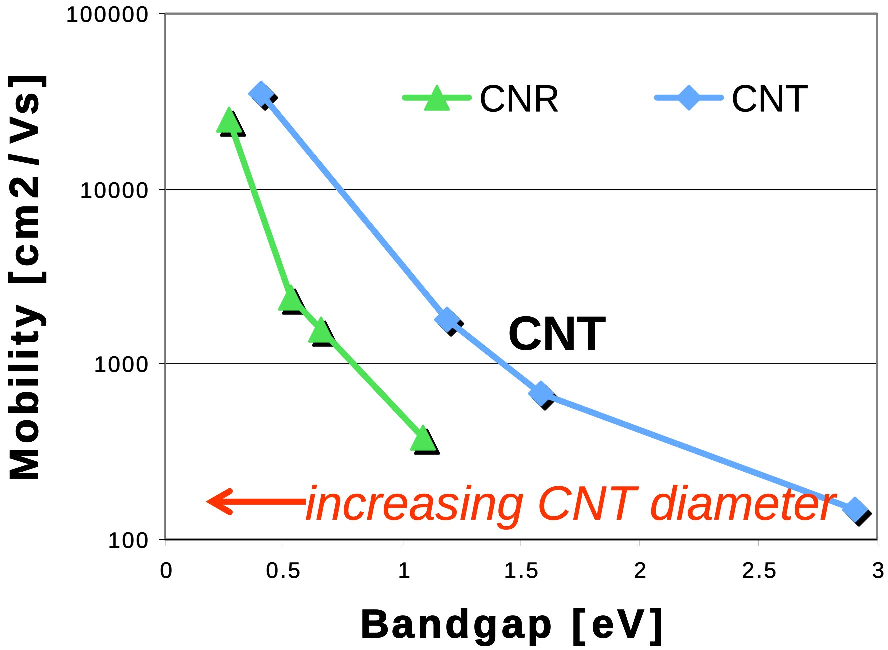




- **Device performance of CNT depends on tube diameter**
- **High-performance of CNT may come at the expense of high device off-state leakage (energy bandgap related ?)**

Emerging Device: Carbon Nanotube Transistor

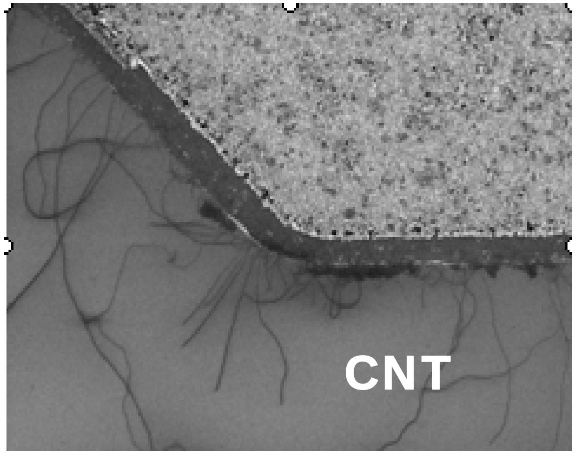


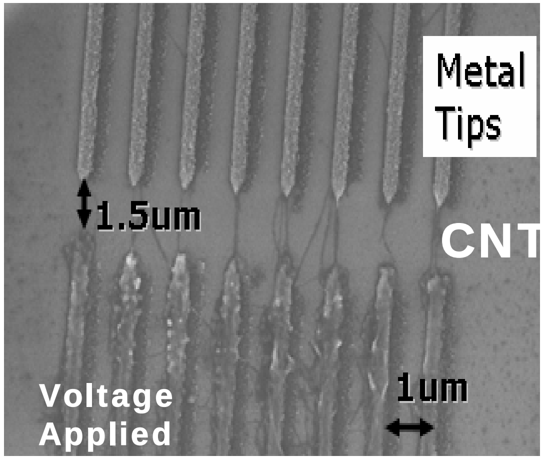


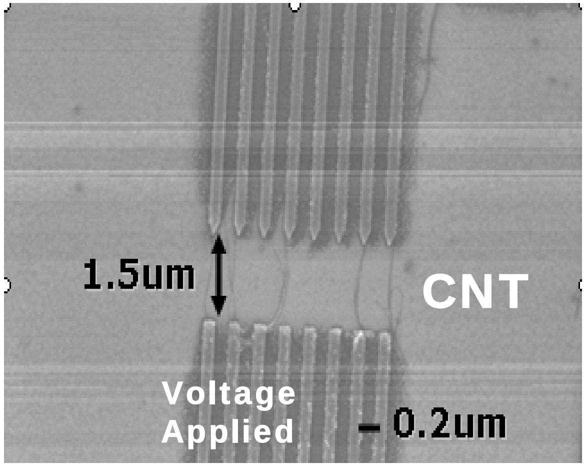
Source: B. Obradovic, R. Kotlyar, *et al*, Applied Physics Letters, 88, 142102 (2006).

- **Performance and leakage related to CNT diameter, which is related to energy bandgap**
- **Analogous to low-bandgap/high-mobility III-V devices which require quantum-well device structures ?**

Fundamental Issue for CNT: Assembly Problem

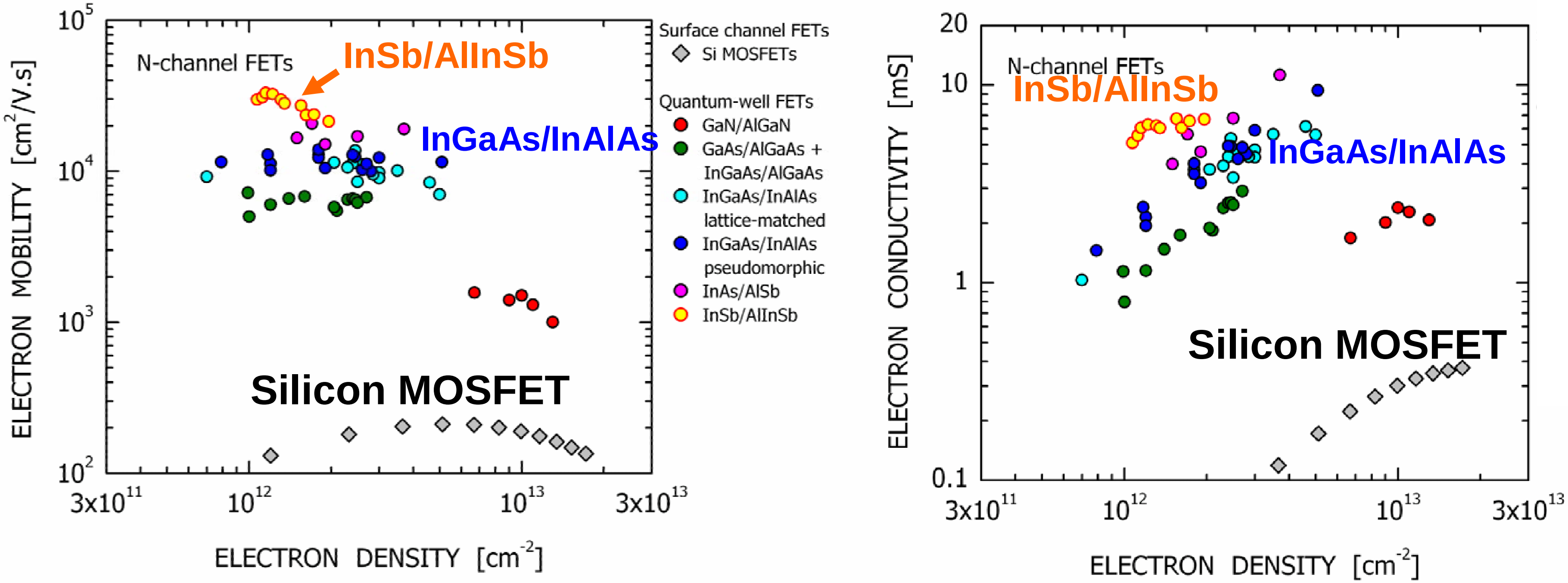






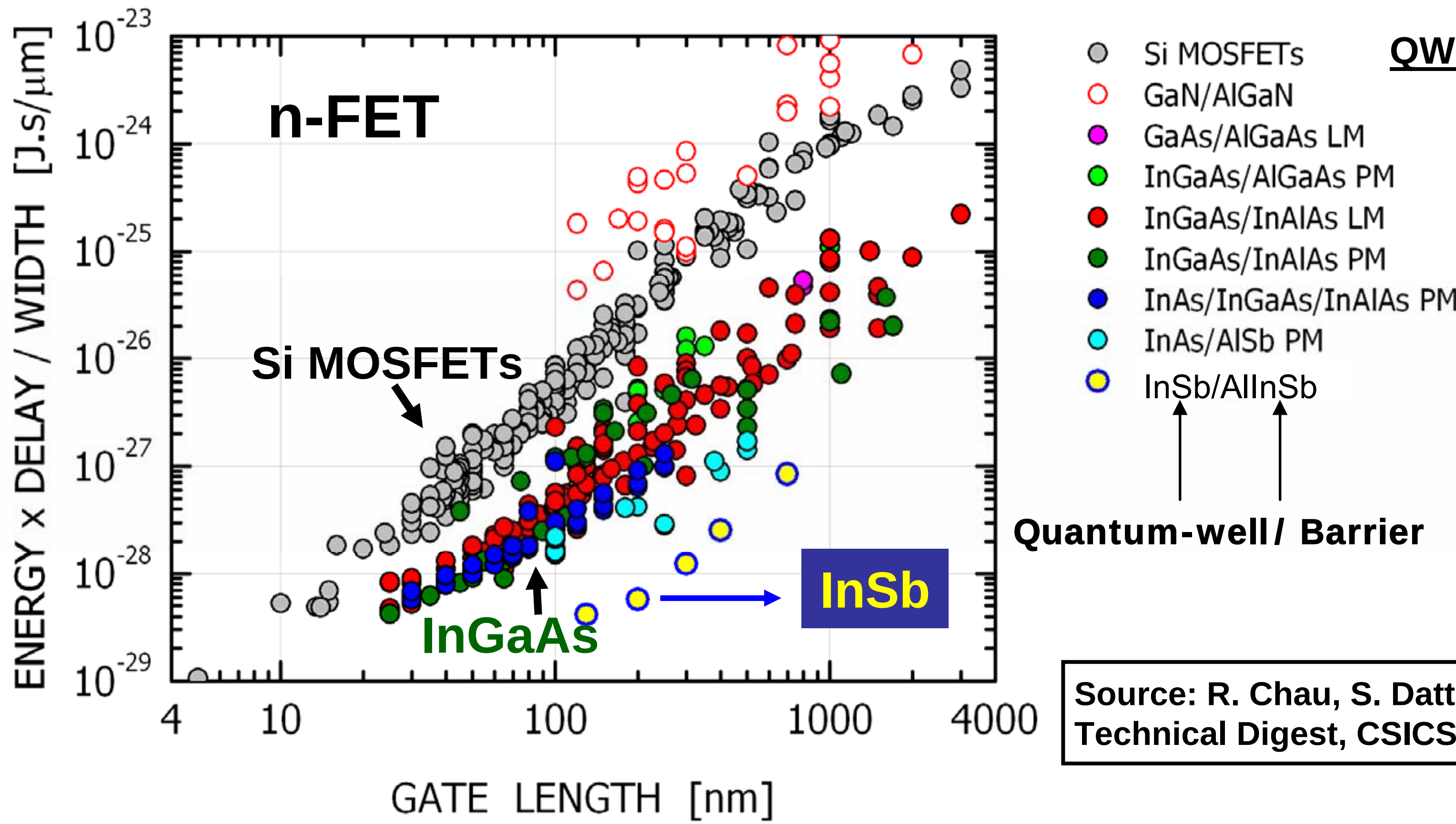
- **Good progress has been made in assembling bottom-up chemically synthesized electronic materials (e.g. CNT)**
- **Still many problems to solve before transistor arrays can be made for VLSI**

Why III-V Research for Future Logic Applications?



- **III-V has been used in commercial communication & optoelectronics products for a long time**
- **III-V quantum-wells show ~100X higher electron mobility and ~20X higher electron conductivity than Si ➔ [potentially high-speed + low-power]**
- **Top-down patterning as opposed to bottom-up chemical synthesis**
- **III-V will NOT replace Si; it will need to be integrated onto Si**

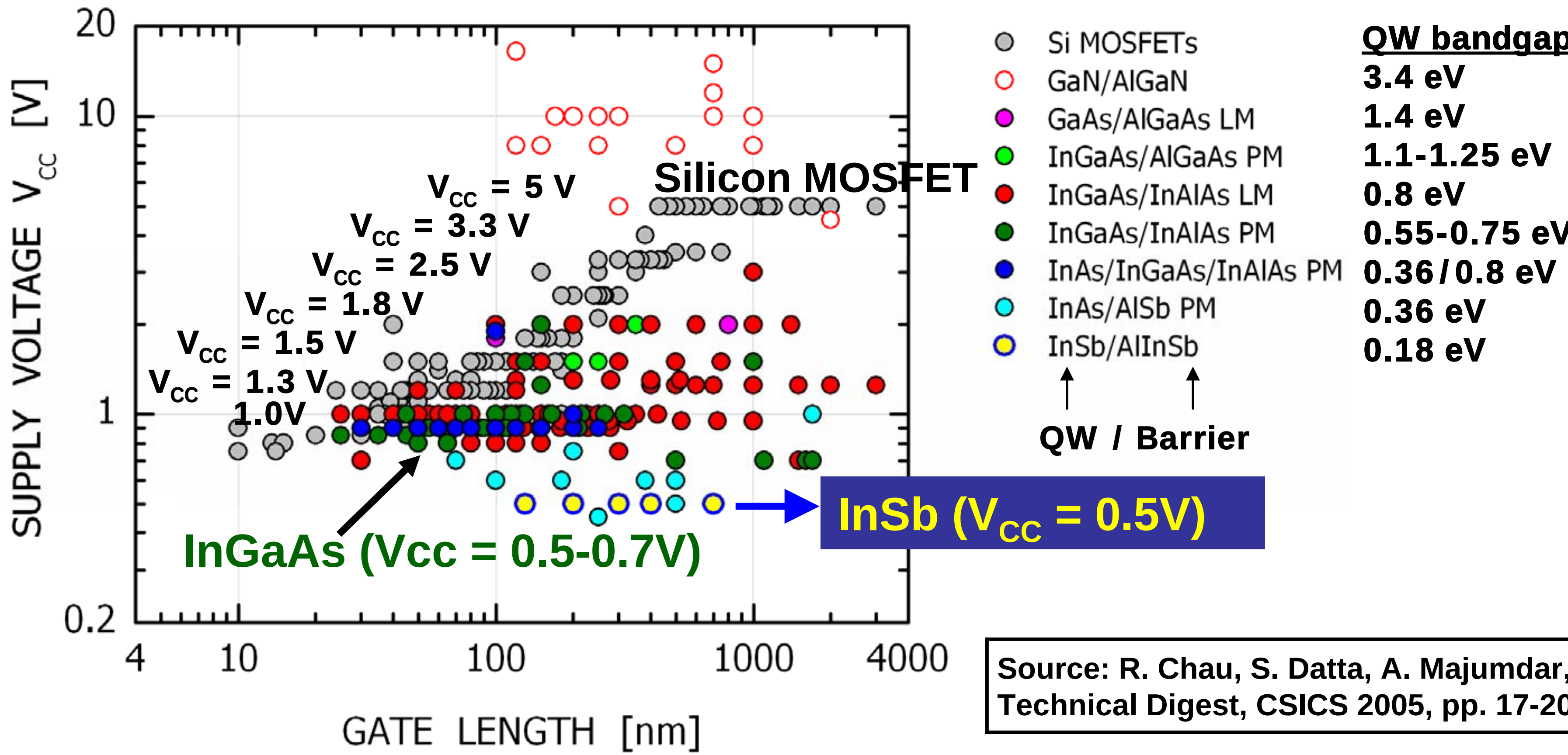
III-V Nanoelectronics: Low Energy-Delay Product



Source: R. Chau, S. Datta, A. Majumdar, Technical Digest, CSICS 2005, pp. 17-20

- Of all the III-V quantum-well systems, InSb QW has the lowest energy-delay product [highest electron mobility, lowest band gap, lowest V_{CC} (0.5V)]
- InGaAs QW is also important for low V_{CC} (0.5V-0.7V)

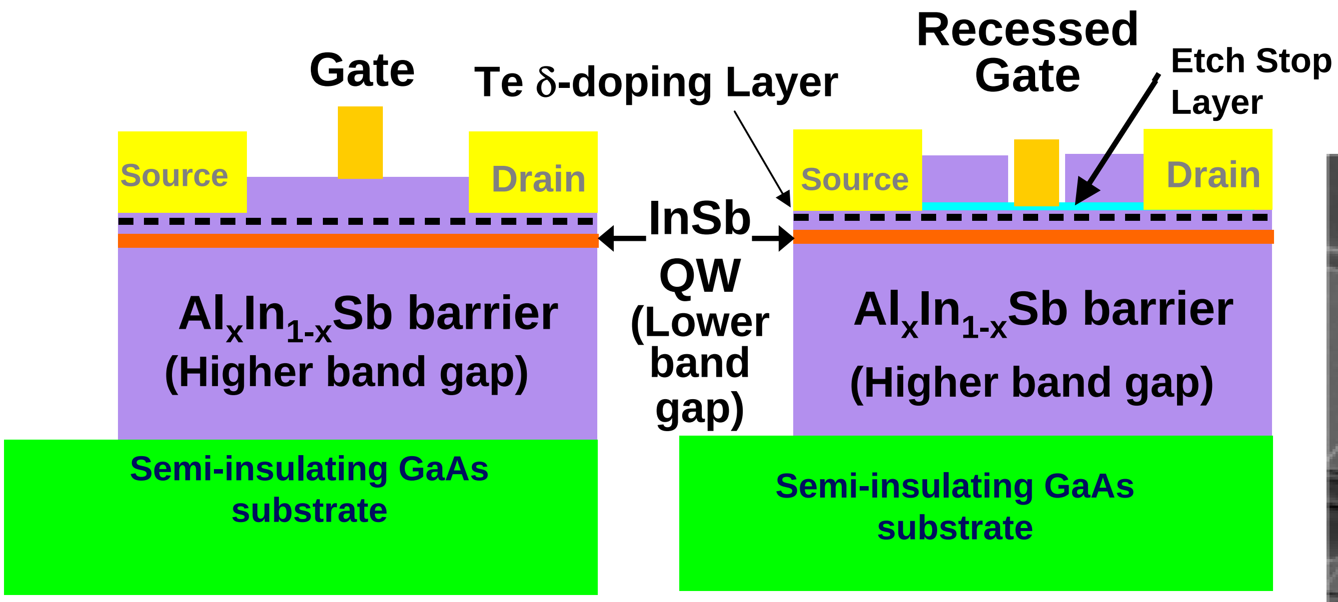
III-V Nanoelectronics Enables Low V_{CC}

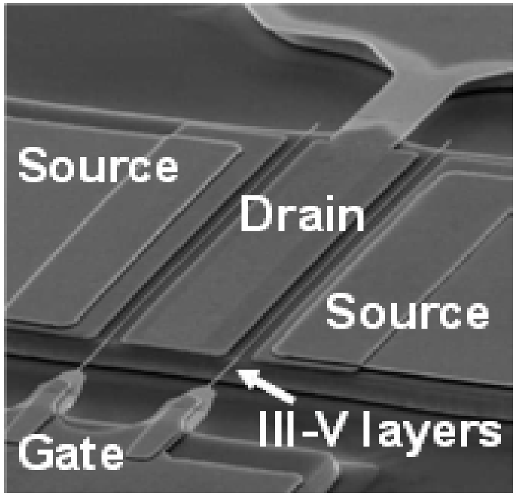


Source: R. Chau, S. Datta, A. Majumdar, Technical Digest, CSICS 2005, pp. 17-20

- **Low bandgap and high mobility in III-V QW's enable low V_{CC} applications**

Example of III-V Quantum-Well Transistor





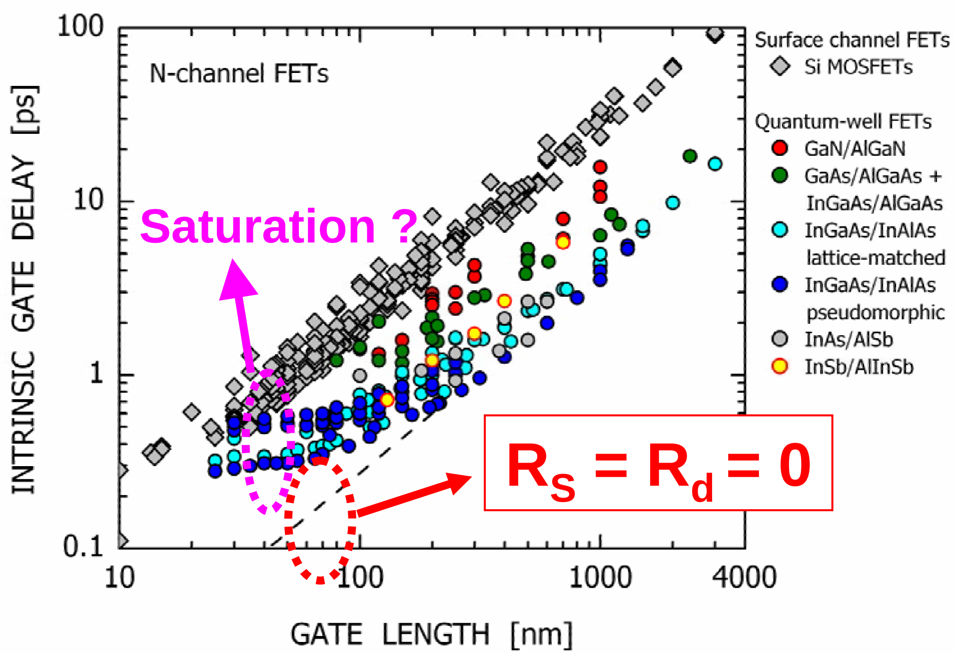
Depletion mode (Normally ON)

Enhancement mode (Normally OFF)

Source: Intel and QinetiQ
ICSICT 2004, IEDM 2005

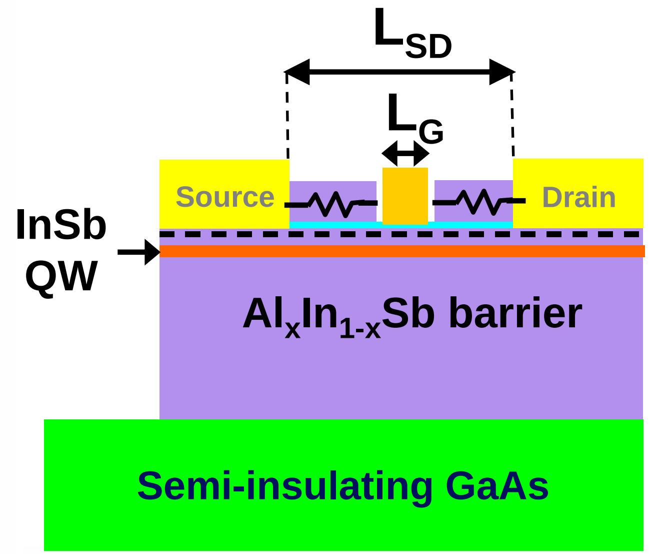
- Quantum-well to reduce parasitic junction leakage and I_{OFF}
- At present Schottky metal gates are used without gate dielectric …… high parasitic gate leakage current

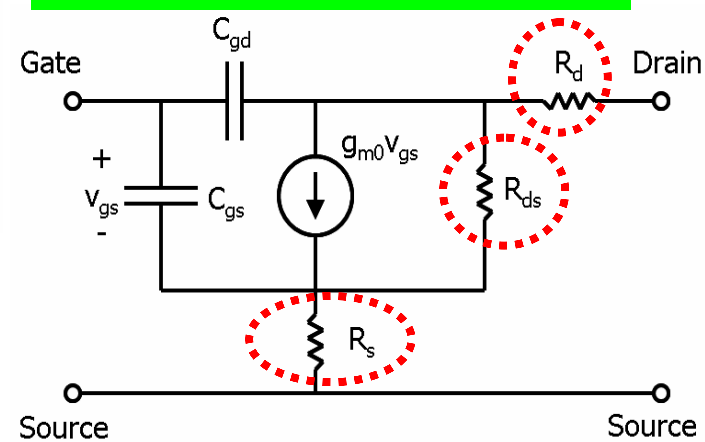
Intrinsic Speed vs Device Gate Length vs Source/Drain Resistance



Source: R. Chau, S. Datta, A. Majumdar, Technical Digest, CSICS 2005, pp.17-20

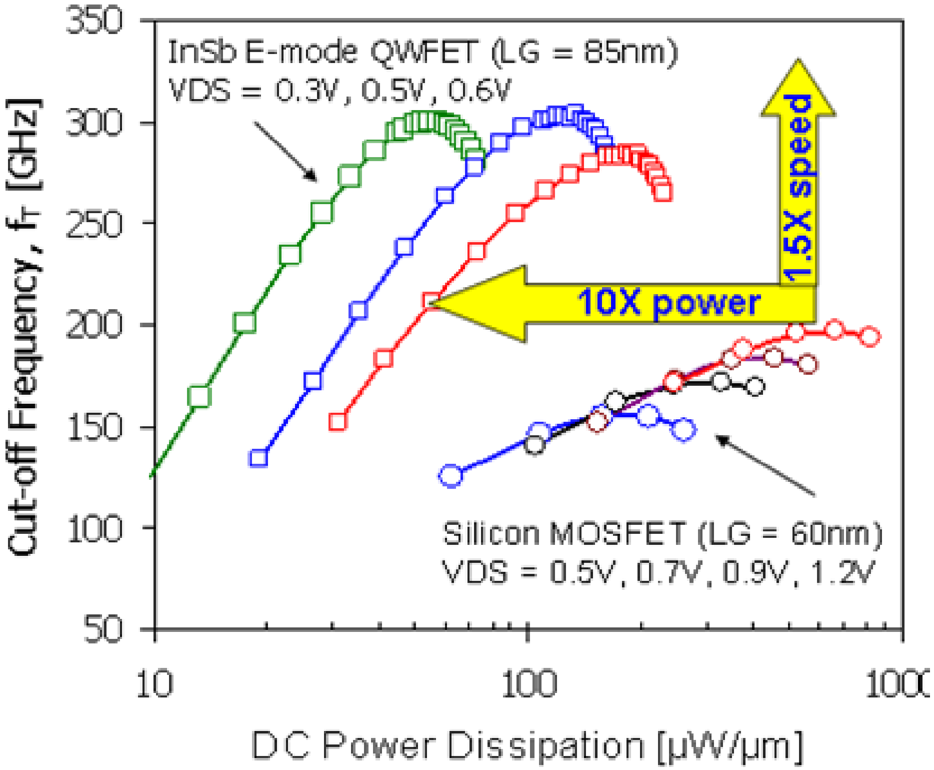
- **Reducing parasitic source and drain resistances (R_S and R_d) will improve intrinsic speed with L_G scaling**

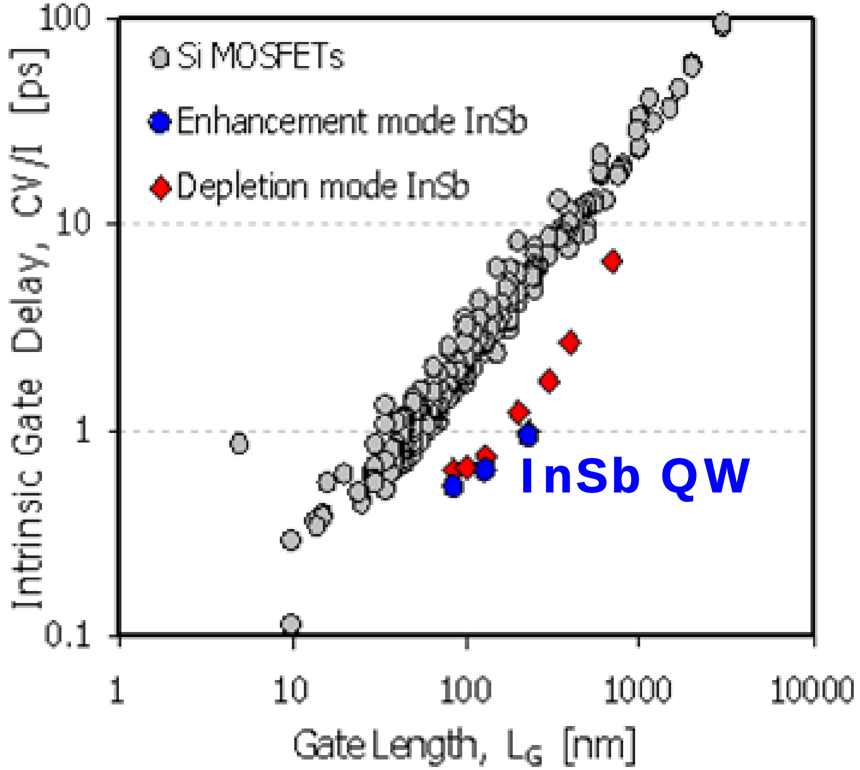




$$f_T = \frac{1}{2\pi}\frac{g_{m0}}{(C_{gs}+C_{gd})\left[1+\frac{R_s+R_d}{R_{ds}}\right]+C_{gd}g_{m0}(R_s+R_d)}$$

Potentially Useful for Future High-Speed and Low-Power Applications

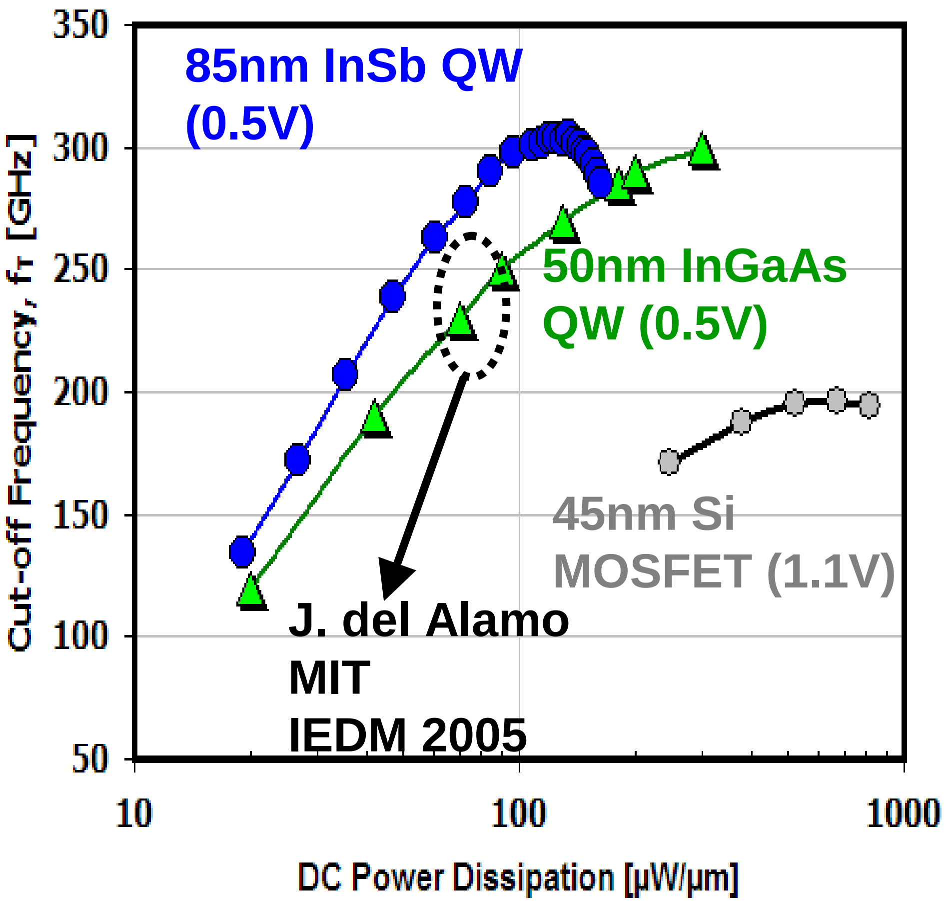


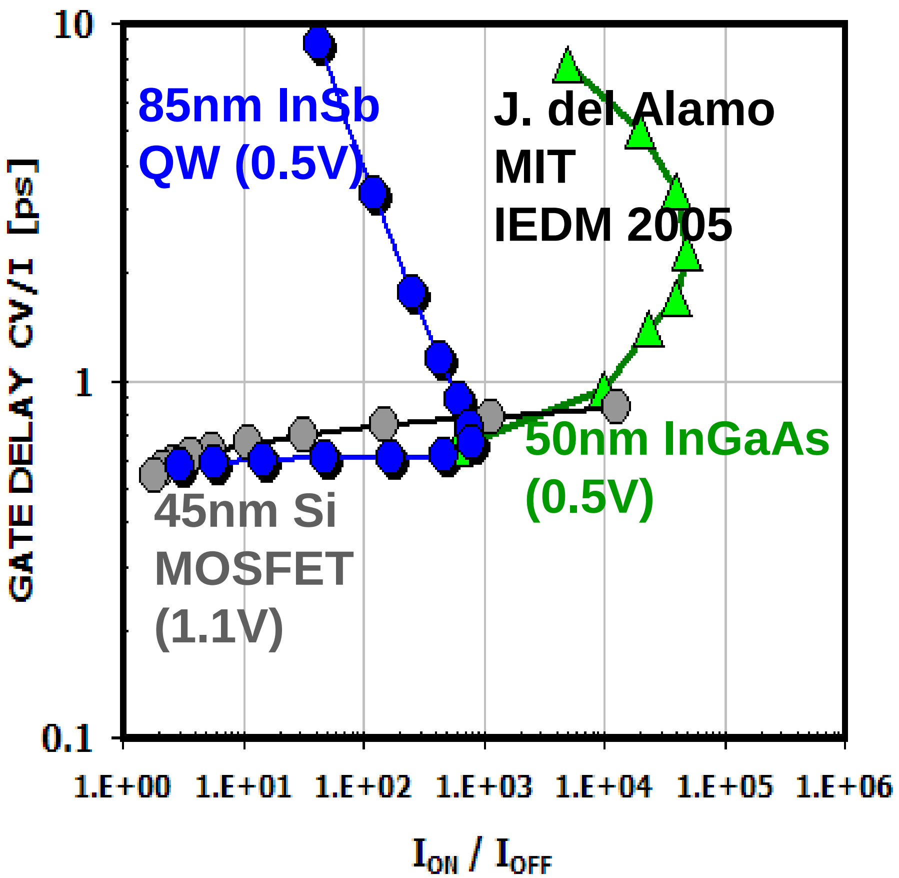


Source: Intel and QinetiQ, IEDM 2005

- **InSb QW shows high performance at low V_{CC} (>300 GHz at 0.5V)**

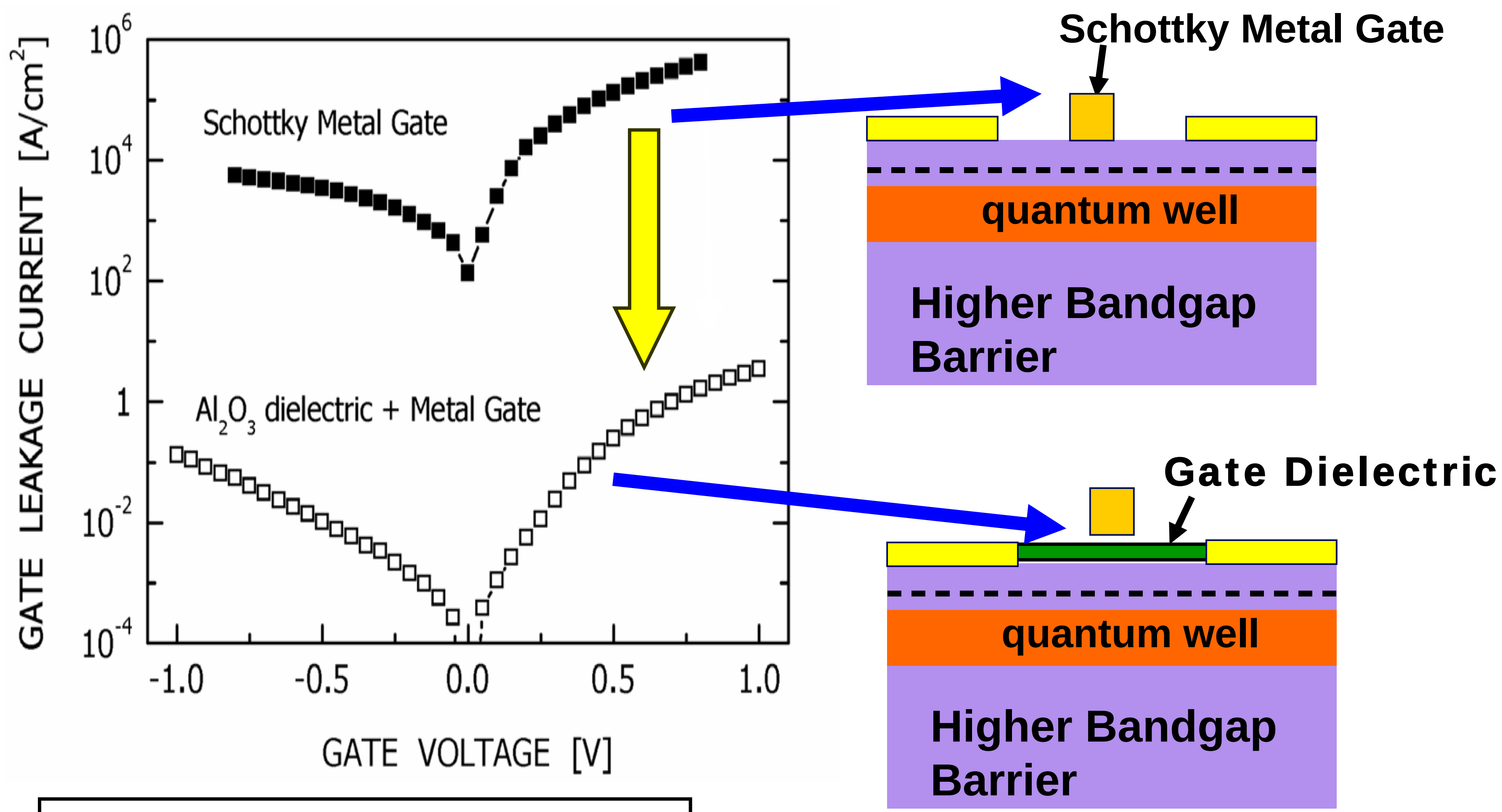
Potentially Useful for Future High-Speed and Low-Power Applications





- InSb QW has the highest performance because of the highest mobility; InGaAs QW also shows high performance at 0.5V

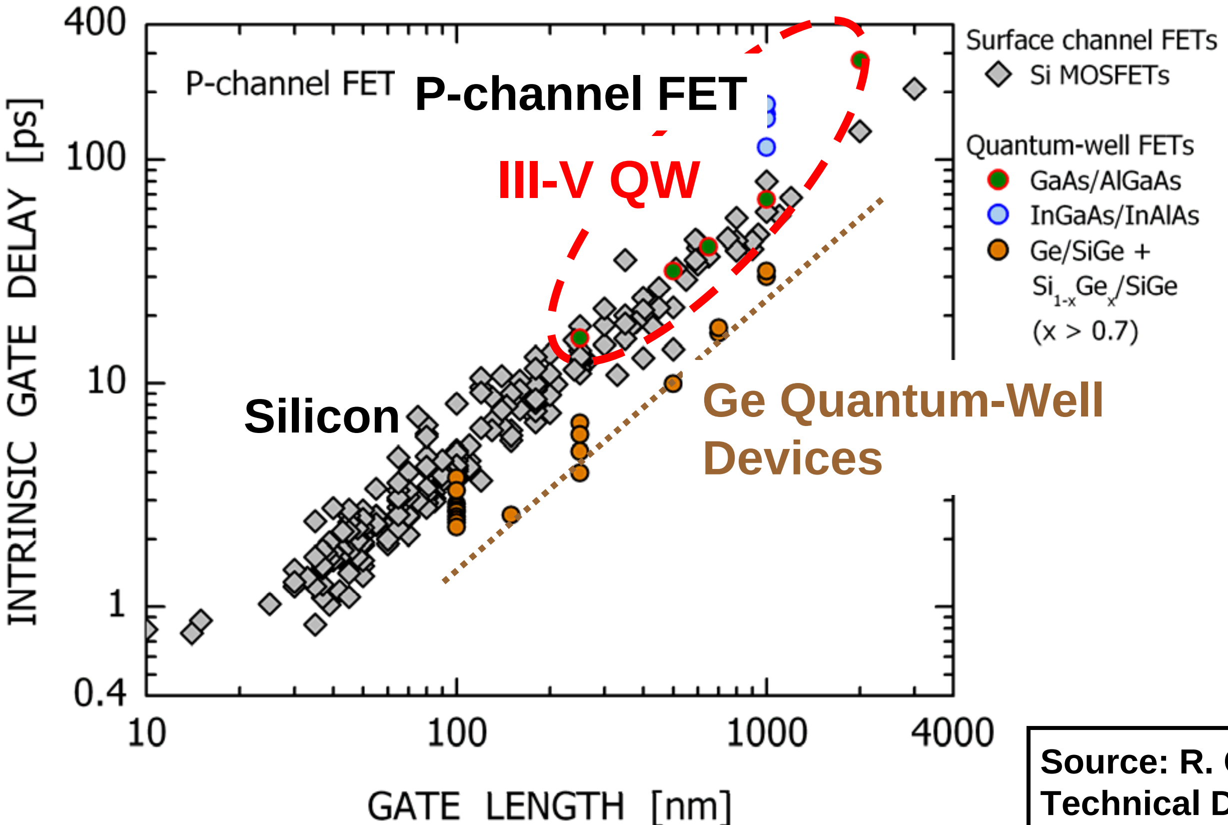
Parasitic Gate Leakage due to Schottky Gate



Source: Intel and QinetiQ, IEDM 2005

- Gate dielectric required to reduce the parasitic gate leakage

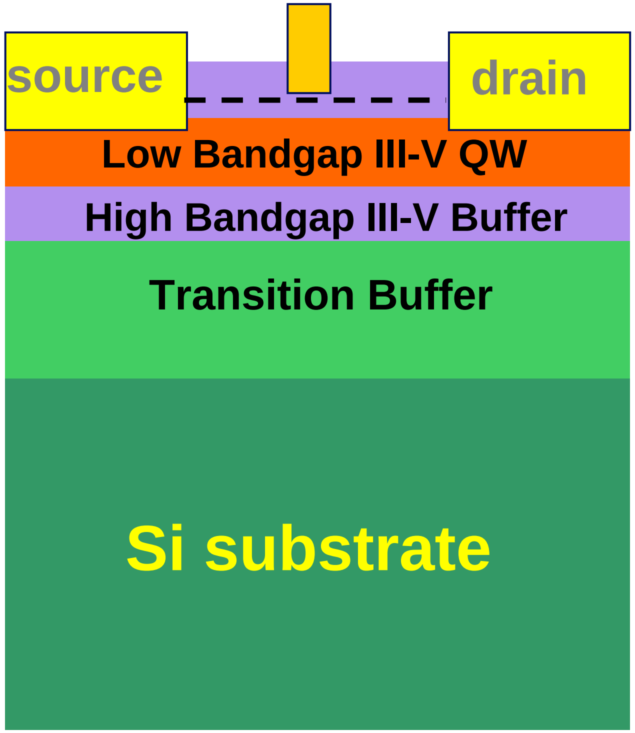
How About Hole Mobility and P-ch FET ?



Source: R. Chau, S. Datta, A. Majumdar, Technical Digest, CSICS 2005, pp. 17-20

- **III-V materials show hole mobility comparable to Si**
- **Improve hole mobility in III-V via compressively strained III-V quantum wells and/or other means (???)**
- **Find the right p-ch FET using other materials for the CMOS (?)**

Integration of III-V on Si



- **Issues/Challenges**
  - Large lattice mismatch
  - Polar/non-polar mismatch → anti-phase domain
  - Thermal mismatch

Challenges

- **Stable and reliable gate dielectrics for III-V**
- **Integration of III-V on Si**
- **PMOS solution to the CMOS configuration**
- **New logic/memory circuits and architecture (?)**

Opportunities

- **Very high-speed circuits at low supply voltage (e.g. 0.5V) for future computation applications**
- **III-V on silicon to enable new functionalities on silicon and also new applications**